The Office Action has rejected Claims 3, 7-9 under 35 U.S.C. §103(a) as being unpatentable over Ziegler. The Office Action has rejected Claims 10, 12 and 13 under 35 U.S.C. §103(a) as being unpatentable over Ziegler in view of Handy "The Cache Memory Book" ("Handy"). The Office Action has rejected Claim 11 under 35 U.S.C. §103(a) as being unpatentable over Ziegler in view of "Handy", in further view of Islam et al. US Patent 6,032,228 ("Islam"). The Office Action has rejected Claims 14-16 under 35 U.S.C. §103(a) as being unpatentable over Ziegler in view of Islam.

Summary of Applicant's Invention

The present invention provides a **peripheral device interface control chip** having a cache system therein for synchronization data communication with external devices. The cache system inside the control chip is capable of reducing latency period when data are read by a peripheral device, so that utilization of the peripheral device and the peripheral device bus is increased. Furthermore, correctness of transmitted data is further ensured through a data synchronization method. "The peripheral device interface control chip having a cache system in a computer system. The computer system includes a set of memory units, a central processing unit (CPU), a CPU bus, a peripheral device bus and at least one peripheral device. The **cache system** includes **a data buffer** and **a peripheral device interface controller.** The **data buffer is located within the control chip** for holding a data stream read from the memory so that data required by the peripheral device are provided." *See SPECIFICATION Page 4, Lines 1-6.* **"The peripheral device controller is also installed within the control chip.** The controller is used for **determining** if the data stream includes data demanded by a particular peripheral device, **determining** if the data stream is synchronous to the data in the corresponding address, retrieving the data stream from memory and putting the data in a data buffer, and **switching** the state of that portion of the data buffer having data stream therein." *See SPECIFICATION Page 4, Lines 11-16.*

Discussion of Office Action Rejections

I. Claims 1, 2, 4-6 Rejected Under 35 U.S.C. §102(e)

The Office Action has rejected Claims 1, 2, 4-6 under 35 U.S.C. §102(e) as being anticipated by Ziegler et al US Patent 6,182,176 ("Ziegler"). Applicant has carefully reviewed the reference and respectfully disagrees.

In response thereto, please consider following reasons and withdraw the rejections.

Ziegler teaches a flow control mechanism for a computer system that handles multiple transactions that cannot all be processed immediately without imposing unnecessary delays. *See Col. 3, Lines 22.* "The bus system also has a bus controller that has means for limiting the types of transactions sent on the bus. When a queue in one of the modules has less than a predetermined amount of free space, the bus controller limits transactions that may be sent on the bus so as to prevent transactions requiring space in that queue from being issued. *See Col. 3, Lines 44-50.* "...main memory controller 14 may be considered the "host" module and the remaining components may be considered "client modules." The main memory controller/host module sends client option signals to each client module specifying the types of transactions, if any, permitted on the bus during a given cycle. The bus owner during a given cycle can only initiate transactions of a type permitted by the client option signal governing that cycle. The bus owner during the next available cycle is also determined by arbitration based on the client option signals, along with arbitration signals from each of the client modules, and a signal sent by the current bus owner indicating whether it needs to return control of the bus." *See Col. 5, Line 59 - Col.6, Line 4.* "....main memory controller 14 preferably also serves as the host module for purposes of bus control. Main memory controller 14 controls a CLIENT_OP line 40, which is coupled directly to each client module. Main memory controller 14 sends signals to each client module on CLIENT_OP line 40 to indicate what types of transactions may be placed on bus 12 during the next available bus cycle." *See Col. 6, Lines 29-34.*

Claim 1 of Applicant's invention recites:

> 1. A cache system inside the ***peripheral device interface control chip*** of a computer system that includes a memory unit, a central processing unit (CPU), a CPU bus, a peripheral device bus and at least one peripheral device, comprising:
>
> a data buffer located within the control chip for holding a data stream read from the memory unit so that data required by the peripheral device bus are provided, and when the data stream is synchronous with data in a corresponding address within the memory unit, the data stream is retained, and ***when any one of the peripheral devices demands data already in the data stream, data within the data stream can be immediately provided by the data buffer so a latency period for retrieving the data stream from memory again is reduced***; and
>
> a peripheral device interface controller ***installed within the control chip for determining if*** the data stream includes data demanded by a particular peripheral device and ***determining if*** the data stream is synchronous with data in the corresponding address, then retrieving the data stream from the memory unit and putting the data in a data buffer, and ***finally switching a state*** of that portion of the data buffer having data stream therein.

(Emphasis added). Applicant respectfully submits that claim 1 patently defines over the cited prior art for at least the reason that the cited reference fails to teach at least those features emphasized above.

A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference. *Verdegaal Bros. v. Union Oil Co. of California, 814 F.2d 628, 631, 2USPQ2d, 1051, 1053 (Fed. Cir. 1987).*

More specifically, the Office Action stated that Ziegler discloses the "cache system inside the peripheral device interface control chip" of a computer system. The Applicants do not agree with such assertions and respectfully traverse the rejection. The Ziegler does not disclose, either expressly or inherently described, "***a peripheral device interface controller installed within the control chip for determining if*** the data stream includes data demanded by a particular peripheral device and ***determining if*** the data stream is synchronous with data in the corresponding address, then retrieving the data stream from the memory unit and putting the data in a data buffer, and ***finally switching a state*** of that portion of the data buffer having data stream therein", as addressed in claim 1. The Ziegler does not disclose, either expressly or

inherently described, "*.....when any one of the peripheral devices demands data already in the data stream, data within the data stream can be immediately provided by the data buffer so a latency period for retrieving the data stream from memory again is reduced*" as addressed in claim 1.

Instead, the Ziegler discloses a flow control mechanism handling multiple transactions that cannot all be processed immediately without imposing unnecessary delays. The **main memory controller 114 for the Main Memory 115** is considered the "host" module and the remaining components may be considered "client modules." **The main memory controller/host module 114 sends client option signals to each client module specifying the types of transactions**, if any, permitted on the bus during a given cycle. The bus owner during a given cycle can only initiate transactions of a type permitted by the client option signal governing that cycle. **The bus owner during the next available cycle is also determined by arbitration based on the client option signals**, along with arbitration signals from each of the client modules, and a signal sent by the current bus owner indicating whether it needs to return control of the bus." *See Col. 5, Line 59 - Col.6, Line 4.* The main memory controller 114 is not installed in the "***peripheral device interface control chip***" as defined in claim 1. The main memory controller 114 acts as a "host module" and arbitrate the transactions on the bus for each cycle. The Ziegler does not disclose, either expressly or inherently described, a peripheral device interface controller ***installed within the control chip for determining if*** the data stream includes data demanded by a particular peripheral device and ***determining if*** the data stream is synchronous with data in the corresponding address, and ***finally switching a state*** of that portion of the data buffer having data stream therein, as addressed in claim 1.

Thus, Ziegler does not anticipate claim 1, and the rejection should be withdrawn. If independent claim 1 is allowable over the prior art of record, then its dependent claims 2, 4-6 are allowable as a matter of law, because these dependent claims contain all features and elements of their respective independent claim 1. *In re Fine*, 837 F.2d 1071 (Fed. Cir. 1988). Additionally and notwithstanding the foregoing reasons for the allowability of claim 1, these dependent claims recite further features/steps and/or

combinations of features/steps (as is apparent by examination of the claims themselves) that are patentably distinct from the prior art of record.

The rejection of claims 1, 2 and 4-6, therefore, should be withdrawn.

II. Claims 3, 7-9 Rejected Under 35 U.S.C. §103(a)

The Office Action has rejected Claims 3, 7-9 under 35 U.S.C. §103(a) as being unpatentable over Ziegler.

Incorporated reasons of independent claim 1 being distinguished over Ziegler set forth above, the claim 1 is allowable over the prior art of record, then its dependent claims 3, 7-9 are allowable as a matter of law, because these dependent claims contain all features and elements of their respective independent claim 1. *In re Fine*, 837 F.2d 1071 (Fed. Cir. 1988). Additionally and notwithstanding the foregoing reasons for the allowability of claim 1, these dependent claims recite further features/steps and/or combinations of features/steps (as is apparent by examination of the claims themselves) that are patentably distinct from the prior art of record. Hence, there are other reasons why these dependent claims are allowable.

Regarding claim 3, it recites:

> 3. The cache system of claim 1, wherein the peripheral device interface controller further includes **receiving signals emitted when data are written from the peripheral device bus to the corresponding address.**
> *(Emphasis added)*

In making the rejection, the Office Action correctly acknowledges that Ziegler neither discloses nor suggests the peripheral device interface controller includes **receiving signals emitted when data are written from the peripheral device bus to the corresponding address.** However, the Office Action asserted that it is well known in the art the necessity indicating the completion of an I/O operation. The Office Action further indicated that two primary means of "assertion of an signal" and "assertion of a special status register", both of which communicating the writing of data from the

peripheral device bus to a corresponding address involve the assertion of signal. The Office Action concluded that it would have been obvious to one having ordinary skill in the art at the time the invention was made to use a signal emitted when data is written from the peripheral device bus to the corresponding address for the purpose of notifying the action's completion. The applicant respectfully disagrees.

Ziegler failed to disclose, teach, or even suggest the peripheral device interface controller including the feature of receiving signals emitted when data are written from the peripheral device bus to the corresponding address. On the contrary, Ziegler teaches a flow control mechanism for a computer system that handles multiple transactions that cannot all be processed immediately without imposing unnecessary delays. *See Col. 3, Lines 22.* "The bus owner during a given cycle can only initiate transactions of a type permitted by the client option signal governing that cycle. The bus owner during the next available cycle is also determined by arbitration based on the client option signals, along with arbitration signals from each of the client modules, and a signal sent by the current bus owner indicating whether it needs to return control of the bus." *See Col. 5, Line 59 - Col.6, Line 4.* There is no requisite teaching, suggestion or motivation to combine the teachings of means of "assertion of an signal" and "assertion of a special status register" in the art with the Ziegler. It is therefore asserted that, as a whole, no combination of the teachings of the cited references could render obvious the invention as recited in claim 3.

Regarding claim 8, it recites:

> 8. The cache system of claim 7, wherein the eight lines are divided into four transmission blocks each having two lines.

The Office Action asserted, on *Page 6, Lines 10-11*, that "Ziegler does not disclose the exact means of placement of data within a cache block suggesting a plurality of **possible schemes**" and concluded that it would have been obvious to one having ordinary skill in the art at the time the invention was made to use all possible schemes to have the eight lines divided into four transmission blocks for the purpose of reducing the complexity of placement logic. The applicant respectfully disagrees.

Obviousness cannot be established by combining the teachings of the prior art to produce the claimed invention, absent some teaching or suggestion supporting the combination. Under section 103, teachings of references can be combined only if there is some suggestion or incentive to do so." Although couched in terms of combining teachings found in the prior art, the same inquiry must be carried out in the context of a purported obvious "modification" of the prior art. The mere fact that the prior art may be modified in the manner suggested by the Examiner does not make the modification obvious unless the prior art suggested the desirability of the modification, In re Fritch 23 USPQ2d 1784.

There is no requisite teaching, suggestion or motivation to combine the teachings of means of "assertion of an signal" and "assertion of a special status register" in the art with the Ziegler. The reason of "Ziegler does not disclose the exact means of placement of data within a cache block" does not provide such desirability of the modification.

The rejection of claims 3 and 7-9, therefore, should be withdrawn.

III. Claims 10, 12 and 13 rejected under 35 U.S.C. §103(a) as being unpatentable over Ziegler in view of Handy

The Office Action has rejected Claims 10, 12 and 13 under 35 U.S.C. §103(a) as being unpatentable over Ziegler in view of Handy "The Cache Memory Book" ("Handy").

In making the rejection, the Office Action correctly acknowledges that Ziegler neither discloses nor suggests a control chip includes a peripheral device interface controller and a data buffer and the central processing unit uses a MOESI protocol, and "when the cache data stream is in a modified state and if the data buffer executes a read operation from an address in memory that corresponds to the cache data stream, the peripheral device interface controller inform the central processing unit to set the cache data stream into an owner state; and when the cache data stream is in an exclusive state and if the data buffer executes a read operation from the corresponding

address, the peripheral device interface controller will inform the central processing unit to set the cache data stream into a shared state" as addressed in claim 10.

It is undisputed that "[t]he PTO has the burden under section 103 to establish a prima facie case of obviousness. It can satisfy this burden only by showing some objective teaching in the prior art or that knowledge generally available to one of ordinary skill in the art would lead that individual to combine the relevant teachings of the references." In re Fine, 837 F.2d 1071, 5 U.S.P.Q.2d 1596, 1598 (Fed. Cir. 1988) (Citations omitted). In particular, "[i]t is impermissible within the framework of section 103 to pick and choose from any one reference only so much of it as will support a given position, to the exclusion of other parts necessary to the full appreciation of what such reference fairly suggests to one of ordinary skill in the art." In re Wesslau, 353 F.2d 238, 147 U.S.P.Q. 391, 393 (C.C.P.A. 1965).

Based on the foregoing propositions of law and applying those propositions to the pending rejections, Applicants respectfully assert that the primary reference, i.e., Ziegler, either individually or in combination with the other asserted references, is legally deficient for the purpose of rendering the claimed invention obvious. In this regard, the following is provided to reemphasize several features of the present invention.

Regarding claim 10, it recites:

> 10. A method of synchronization data transmission between cache memory inside a peripheral device interface control chip and external device that can be applied to a computer system having a memory unit, at least one central processing unit, a control chip, a peripheral device bus, a CPU bus and at least one peripheral device, wherein the control chip includes a peripheral device interface controller and a data buffer and the central processing unit uses a MOESI protocol, a memory data stream becomes a cache data stream when the memory data stream within the memory is read into the central processing unit, and the memory data stream becomes a buffer data stream when the memory data stream is read into the data buffer, further comprising the steps wherein:
>
> when the cache data stream is in a modified state and if the data buffer executes a read operation from an address in memory that corresponds to the cache data stream, ***the peripheral device interface controller inform the central processing unit*** to set the cache data stream into an owner state; and
>
> when the cache data stream is in an exclusive state and if the data buffer executes a read operation from the corresponding address, ***the peripheral device***

interface controller will inform the central processing unit to set the cache data stream into a shared state.

(Emphasis added)

Either of the references, Ziegler and Handy, applied against claim 10, along or in combination, shows or suggests (1) when the cache data stream is in a modified state and if the data buffer executes a read operation from an address in memory that corresponds to the cache data stream, ***the peripheral device interface controller inform the central processing unit*** to set the cache data stream into an owner state; (2) when the cache data stream is in an exclusive state and if the data buffer executes a read operation from the corresponding address, ***the peripheral device interface controller will inform the central processing unit*** to set the cache data stream into a shared state.

The Office Action asserted that "With the MOESI protocol implemented within Ziegler this would lead to informing the central processing unit to set the cache data stream into an owner state informing the central processing unit when the cache data stream is in a modified state and if the data buffer executes a read operation from an address in memory that corresponds to the cache data stream, and ; and informing the central processing unit to set the cache data stream into a shared state when the cache data stream is in an exclusive state and if the data buffer executes a read operation from the corresponding address."

Although couched in terms of combining teachings found in the prior art, the same inquiry must be carried out in the context of a purported obvious "modification" of the prior art. The mere fact that the prior art may be modified in the manner suggested by the Examiner does not make the modification obvious unless the prior art suggested the desirability of the modification, In re Fritch 23 USPQ2d 1784.

Ziegler teaches a flow control mechanism for a computer system that handles multiple transactions that cannot all be processed immediately without imposing unnecessary delays. The bus owner during a given cycle can only initiate transactions of a type permitted by the client option signal governing that cycle. The bus owner

during the next available cycle is also determined by arbitration based on the client option signals, along with arbitration signals from each of the client modules, and a signal sent by the current bus owner indicating whether it needs to return control of the bus. By arbitration, the flow control mechanism for handling multiple transactions from different "client modules" can be processed without unnecessary delays.

There is no requisite teaching, suggestion or motivation to combine the teachings of means of "MOESI protocol" in the Handy with the Ziegler to render claim 10 obvious to people of ordinary skill in the art. Furthermore, either of the references applied against claim 10, along or in combination, shows or suggests "***the peripheral device interface controller inform the central processing unit*** to set the cache data stream into an owner state or a shared state, as addressed in claim 10.

The rejection of claim 10, therefore, should be withdrawn.

Incorporated reasons of independent claim 10 being distinguished over Ziegler in view of Handy set forth above, the claim 10 is allowable over the prior art of record, then its dependent claims 12 and 13 are allowable as a matter of law, because these dependent claims contain all features and elements of their respective independent claim 10. *In re Fine*, 837 F.2d 1071 (Fed. Cir. 1988). Additionally and notwithstanding the foregoing reasons for the allowability of claim 10, these dependent claims recite further features/steps and/or combinations of features/steps (as is apparent by examination of the claims themselves) that are patentably distinct from the prior art of record. Hence, there are other reasons why these dependent claims are allowable.

Regarding claims 12 and 13, as following recited:

> 12. The data synchronization method of claim 10, wherein a ***probe-hit-read signal is transmitted from the peripheral device interface controller to the central processing unit*** when a buffer data stream is read from the peripheral device interface controller to the data buffer.
>
> 13. The data synchronization method of claim 12, wherein ***the probe-hit-read signal further includes the corresponding addresses.***

(Emphasis added)

Either of the references, Ziegler and Handy, applied against claim 12 and 13, along or in combination, shows or suggests ***the peripheral device interface controller transmitting a probe-hit-read signal to the central processing unit*** to set the cache data stream into an owner state or a shared state. The rejection of claims 12 and 13, therefore, should be withdrawn.

IV. Claim 11 rejected under 35 U.S.C. §103(a) as being unpatentable over Ziegler in view of "Handy", in further view of Islam

The Office Action has rejected Claim 11 under 35 U.S.C. §103(a) as being unpatentable over Ziegler in view of "Handy", in further view of Islam et al. US Patent 6,032,228 ("Islam").

Incorporated reasons of independent claim 10 being distinguished over Ziegler in view of Handy set forth above, the claim 10 is allowable over the prior art of record, then its dependent claim 11 is allowable as a matter of law, because these dependent claims contain all features and elements of their respective independent claim 10.

V. Claims 14-16 rejected under 35 U.S.C. §103(a) as being unpatentable over Ziegler in view of Islam

The Office Action has rejected Claims 14-16 under 35 U.S.C. §103(a) as being unpatentable over Ziegler in view of Islam.

In making the rejection, the Office Action correctly acknowledges that Ziegler neither discloses nor suggests most of the steps addressed in claim 14. The Office Action additionally relies on the teachings of Islam. However, Islam fails to disclose or otherwise suggest all of the state changes as addressed in claim 14, and also admitted in the Office Action on page 15, lines 5-8. Thus, this reference cannot possibly overcome the above-noted deficiencies of Ziegler.

The Islam discloses a "Flexible cache-coherency mechanism." In the cache system, one or more cache components and a set of one or more consistency-replacement functions are provided. A cache component caches one or more items in its one or more cache entries. Items that hit in the cache can result in corresponding cache entries being read or written. Any valid entry in a cache component includes status information reflecting whether the entry has been accessed and whether it has been modified, and is linked to a consistency-action matrix that, in correspondence with the entry's status information and access type (i.e. read or write), determines what consistency action has to be executed in conjunction with the current entry access. Consistency actions and the consistency-action matrix are the inventive mechanisms for implementing cache-coherency and cache-replacement policies.

Ziegler teaches a flow control mechanism for a computer system that handles multiple transactions that cannot all be processed immediately without imposing unnecessary delays. The bus owner during a given cycle can only initiate transactions of a type permitted by the client option signal governing that cycle. The bus owner during the next available cycle is also determined by arbitration based on the client option signals, along with arbitration signals from each of the client modules, and a signal sent by the current bus owner indicating whether it needs to return control of the bus. By arbitration, the flow control mechanism for handling multiple transactions from different "client modules" can be processed without unnecessary delays.

There is no requisite teaching, suggestion or motivation to combine the teachings of means of "Flexible cache-coherency mechanism" in the Islam with the Ziegler to render claim 14 obvious to people of ordinary skill in the art.

Incorporated reasons of independent claim 14 being distinguished over Ziegler in view of Islam set forth above, the claim 14 is allowable over the prior art of record, then its dependent claims 15-16 are allowable as a matter of law, because these dependent claims contain all features and elements of their respective independent claim 14.

The rejection of claims 14-16, therefore, should be withdrawn.

CONCLUSION

For at least the foregoing reasons, it is believe that all pending claims 1-16 are in proper condition for allowance. If the Examiner believes that a conference would be of value in expediting the prosecution of this application, he is hereby invited to telephone the undersigned counsel to arrange for such a conference.

Respectfully submitted,
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